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10/729,092	12/05/2003	Chun-Chieh Lin	TSM03-0670	8814

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/729,092	Applicant(s) LIN ET AL.	
	Examiner Matthew E. Warren	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 13 March 2006.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9,12,14,16,17,22,23,25-34,36-38,40-42,45-55 and 78-80 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9,12,14,16,17,22,23,25-34,36-38,40-42,45-55 and 78-80 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/19/05, 3/13/06.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: also IDS 5/5/06.

DETAILED ACTION

This Office Action is in response to the Amendment filed on March 13, 2006.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 8, 9, 12,14, 16, 17, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr et al. (US Pub. 2004/0262683 A1) in view of Kubo et al. (US 6,674,100 B2).

In re claim 1, Bohr et al. shows (figs. 5-7) a semiconductor structure comprising: a semiconductor substrate that includes a first semiconductor material (115) and a second semiconductor material (470 and 480) wherein the first semiconductor material has a lattice constant that is different from a lattice constant of the second material [0024]; a first transistor (404) formed in the semiconductor substrate, the first transistor having first source and drain regions (204) formed in the substrate oppositely adjacent a first channel region, wherein a first gate dielectric (120) overlies the first channel region and a first gate electrode (132) overlies the first gate dielectric, and wherein the first channel region is formed in the first semiconductor material and at least a portion of the first source and drain regions are formed in the second semiconductor material; the second semiconductor material is only substantially outside a region underlying the first

gate electrode; and a second transistor (403) formed in the semiconductor substrate, having a conductivity type (N type) different than the first transistor, the second transistor having second source and drain regions (203) in the substrate oppositely adjacent a second channel region, wherein a second gate dielectric (120) covers the second channel region and a second gate electrode (130) covers the second gate dielectric. The second semiconductor material comprises silicon (Si) and germanium (Ge) [0024]. Bohr discloses [0037] that the source, drain, and gate electrodes of the first and second transistors each include a silicided portion (523, 513, 524, 514). Bohr does not disclose that the second semiconductor material comprise, Si, Ge, and C. Kubo et al. shows (fig. 1) that an additional semiconductor layer (14p or 14n) may comprises an alloy of silicon, germanium, and carbon. The silicon, germanium, and carbon alloy forms a zone to enhance the electron mobility in the channel region and relax the strain due to lattice misfit between the zone and silicon. The Si, Ge, and C further adjusts the lattice constant so that the layer is matched closely with Si and therefore improves the reliability of the device (col. 4, lines 26-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second semiconductor material of Bohr by using a material comprising silicon, germanium, and carbon as taught by Kubo to adjust the lattice constant to a desired level for relaxing the strain in the substrate and ultimately improving the reliability of the device.

In re claim 8, Bohr discloses [0024] that the lattice constant of the second semiconductor material [470 and 480] is larger than the lattice constant of the first semiconductor material (115).

In re claim 9, Bohr discloses [0024] that the first transistor is a PMOS transistor.

In re claim 12, Kubo discloses (col. 8, line 49-col. 9, line 45) that the concentration of germanium in the SiGe layer is greater than 10%.

In re claims 16 and 17, Kubo discloses (col. 8, line 49-col. 9, line 45) that the semiconductor material comprises silicon, germanium, and carbon. The concentration of carbon is in the range of 0.01 to 0.04 percent.

In re claim 25, none of the references show the specific distance between the junction and gate dielectric edge. It would have been obvious to one of ordinary skill in the art at the time the invention was made to space the first and second semiconductor junction and gate dielectric to a desired distance to arrange the active layer having a specific compressive or tensile stress. It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 2, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr et al. (US Pub. 2004/0262683 A1) in view of Kubo et al. (US 6,674,100 B2) as applied to claim 1 above, and further in view of Currie et al. (US Pub. 2004/0026765 A1).

In re claim 2, Bohr and Kubo show all of the elements of the claims except the first transistor coupled to the second transistor to form an inverter. Currie discloses [0071] that first transistor is coupled to the second transistor to form an inverter. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the device of Bohr and Kubo by connecting the first and second transistors as taught by Currie to form an invert.

In re claim 6, Currie discloses [0075] that the gate dielectric is formed from a high-k dielectric material.

In re claim 7, Currie shows (fig. 3) that the first and second gate electrodes comprise a metal material (352).

Claims 3-5, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable Bohr et al. (US Pub. 2004/0262683 A1) in view of Kubo et al. (US 6,674,100 B2) as applied to claim 1 above, and further in view of Fitzgerald et al. (US Pub. 2002/0125471 A1).

In re claims 3-5, Bohr and Kubo show all of the elements of the claims except the transistor being coupled to form a NOR, NAND, or XOR circuit which Fitzgerald et al. discloses [0125]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the transistors of Bohr and Kubo by coupling them to form NOR, NAND, and XOR circuits as taught by Fitzgerald to provide optimized processing circuits with increased speed.

In re claims 22 and 23, Fitzgerald discloses [0073-0083, 0096] the relationship between the ratios of the gate width and the carrier mobility of the channel.

Claims 26-34, and 36-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akita et al. (US 6,256,239 B1) in view of Currie et al. (US Pub. 2004/0026765 A1) and Kubo et al. (US 6,674,100 B2).

In re claim 26, Akita et al. shows (fig. 11) an inverter comprising; a transistor (Tr_{19}) formed in the semiconductor substrate, the transistor having a source region and a drain region formed in a semiconductor substrate oppositely adjacent a channel region and a load element (13) formed in the semiconductor substrate, the load element coupled between the drain region and a first supply voltage node (Vdd). A second supply voltage node (Vss) is coupled to the source region. Akita et al. shows all of the elements of the claims except the channel being formed in a first semiconductor material and at least a portion of the source region and the drain region is formed in a second semiconductor material, the first semiconductor material being different than the second semiconductor material. Currie et al. shows (fig. 3) a strained transistor having a channel region formed in a first semiconductor layer (311) and portions of source and drain (340) formed in a second semiconductor layer (312). A first gate dielectric (320) overlies the first channel region and a first gate electrode (350A) overlies the first gate dielectric, and the first channel region is formed in the first semiconductor material and at least a portion of the first source and drain regions are formed in the second semiconductor material. A region (312) underlying the gate electrode is substantially free of the first semiconductor material. With such a configuration improved channel performance is provided for both NMOS and PMOS transistors [0064, 0065, 0076]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the transistor channel of the inverter described by Akita by adding different semiconductor materials as taught by Currie to improve the channel performance of the device.

Akita and Currier do not show that the second semiconductor material comprises silicon, germanium, and carbon. Kubo et al. shows (fig. 1) that an additional semiconductor layer (14p or 14n) may comprises an alloy of silicon, germanium, and carbon. The silicon, germanium, and carbon alloy forms a zone to enhance the electron mobility in the channel region and relax the strain due to lattice misfit between the zone and silicon. The Si, Ge, and C further adjusts the lattice constant so that the layer is matched closely with Si and therefore improves the reliability of the device (col. 4, lines 26-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second semiconductor material of Akita and Currier by using a material comprising silicon, germanium, and carbon as taught by Kubo to adjust the lattice constant to a desired level for relaxing the strain in the substrate and ultimately improving the reliability of the device.

In re claims 27-29, Akita discloses that the load element comprises a resistor and the transistor comprises an NMOS or PMOS transistor (col. 6, lines 56-67 and col. 9, lines 11-20). The load element comprises a transistor as shown by the possible load elements in figs. 7(a-d).

In re claim 30, Currie discloses that a strained transistor may be used in an inverter [0071] and improve the channel performance of the device. When combined

with Akita, the strained transistor of Currie would be substituted for the load transistor of Akita to improve the channel performance of that device

In re claims 31 and 32, Currie discloses that a high-k dielectric is used for the gate dielectric [0063] and that the gate electrode comprises metal [0072].

In re claims 33-34, Currie discloses [0014] the well known concept that SiGe has a higher lattice constant than Si. Therefore, the lattice constant of the second semiconductor material (412) is larger than the lattice constant of the first semiconductor material (411) because the second semiconductor material is made of SiGe and the first semiconductor material is made of Si. The first transistor is a PMOS transistor [0077].

In re claim 36, the references do not specifically show that the concentration of germanium is greater than 10%. However, Currie discloses [0065] that a "greater Ge concentration can also enhance hole mobility." It would have been obvious to one of ordinary skill in the art at the time the invention was made to add germanium in any silicon alloy having a desired concentration to enhance hole mobility. It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

In re claim 37, Akita and Currie do not show that the second semiconductor material has a lattice constant smaller than the lattice constant of the first semiconductor material and may comprise, Si, Ge, and C. Kubo et al. shows (fig. 1) that an additional semiconductor layer (14p or 14n) may comprises an alloy of silicon, germanium, and carbon. The silicon, germanium, and carbon alloy forms a zone to

enhance the electron mobility in the channel region and relax the strain due to lattice misfit between the zone and silicon. The Si, Ge, and C further adjusts the lattice constant so that the layer is matched closely with Si and therefore improves the reliability of the device (col. 4, lines 26-45). The lattice constant of a second semiconductor layer may be smaller or greater than the lattice constant of the first semiconductor material, depending on how much Si, Ge, or C is in the layer(col. 10, lines 24-36).

In re claims 38, Currie already shows (fig. 4) that one of the transistors is an NMOS transistor.

In re claim 40, Kubo discloses (col. 8, line 49-col. 9, line 45) that the semiconductor material comprises silicon, germanium, and carbon. The concentration of carbon is in the range of 0.01 to 0.04 percent.

In re claim 41, Currie discloses [0072 and 0078] that the source, drain, and gate electrodes of the first and second transistors each include a silicided portion.

In re claims 42 and 43, Currie shows (fig. 3) that the first semiconductor material (311) consists essentially of silicon (tensile Si) and the second semiconductor (312) material comprises silicon and germanium (SiGe).

In re claim 45, Currie discloses [0016] that the substrate comprises an insulating layer underlying the first semiconductor material to form a SOI device.

In re claim 46, Currie discloses [0072 and 0078] that a conductive material of TaSi is formed over the source and drain regions

In re claims 47-55, Currie shows (fig. 3) that a gate dielectric (320) is formed over the channel and a gate electrode (351) of semiconductor material such as polycrystalline silicon is formed over the gate dielectric. Alternatively the gate electrode may be formed of a metal, silicide, and nitride [0072]. The gate dielectric may also comprise silicon oxide or a high dielectric material such as hafnium oxide [0063].

Claims 78 and 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Currie et al. (US Pub. 2004/0026765 A1) in view of Chen et al. (US 6,891,192, B2) and Kubo et al. (US 6,674,100 B2).

In re claim 78, Currie shows (fig.) a semiconductor structure comprising a semiconductor substrate (460) that includes a first semiconductor material (430), a second semiconductor material (412), and a third semiconductor material (411), wherein the lattice constant of the second semiconductor material is larger than the lattice constant of the first semiconductor material and the lattice constant of the third material is smaller than the lattice constant of the first material. Although Currie does not teach a specific difference in lattice constants, such a limitation is an inherent property of the material. [Mears et al. (US Pub. 2004/0266116 A1) teaches [0008] that the lattice constant of SiGe is larger than Si and is a direct function of the amount of Ge in the SiGe alloy.] Currie discloses [0061] that the relaxed Si-Ge layer (130 or 330 in fig. 4) has a lower concentration of germanium than the compressively strained layer (112 or 412 in fig. 4).Therefore, because the compressively strained Si-Ge layer (112 or 412) of Currie has greater concentration of Ge than the relaxed Si-Ge layer (130 or 33)

or the tensile Si layer (311 with no Ge) then that compressively strained Si-Ge layer (112 or 412 of second semiconductor material) has the highest lattice constant.

A first transistor (300A) is formed in the semiconductor substrate, the first transistor having first source and drain regions (340A) formed in the substrate oppositely adjacent a first channel region. wherein a first gate dielectric (320A) overlies the first channel region and a first gate electrode (350A) overlies the first gate dielectric. The first channel region is formed in the first semiconductor material and at least a portion of the first source and drain regions are formed in the second semiconductor material. A second transistor (300B) is formed in the semiconductor substrate, having a conductivity type (N type) different than the first transistor, the second transistor having second source and drain regions (340B) in the substrate oppositely adjacent a second channel region, wherein a second gate dielectric (320B) covers the second channel region and a second gate electrode (350B) covers the second gate dielectric. At least a portion of the second source and drain regions are formed in the third semiconductor material. Currie shows all of the elements of the claims except the second semiconductor material only substantially outside a region underlying the first gate electrode. Chen et al. shows (fig. 1) that a second semiconductor material (22) of SiGe having a lattice constant different from that of the Si substrate (16) is formed in the source and drain regions and is substantially only outside the region underlying the first gate. By forming the SiGe layer only in the source and drain regions, the electron mobility in the channel is improved without having to forming a thick layer of SiGe. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the second semiconductor layer of Currie by forming it only in the source and drain areas as taught by Chen to improve the electron mobility in the channel without using a thick layer of SiGe.

Currie and Chen do not disclose that the semiconductor material comprises, Si, Ge, and C. Kubo et al. shows (fig. 1) that a semiconductor layer (14p or 14n) may comprises an alloy of silicon, germanium, and carbon. The silicon, germanium, and carbon alloy forms a zone to enhance the electron mobility in the channel region and relax the strain due to lattice misfit between the zone and silicon. The Si, Ge, and C further adjusts the lattice constant so that the layer is matched closely with Si and therefore improves the reliability of the device (col. 4, lines 26-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second semiconductor material of Currie and Chen by using a material comprising silicon, germanium, and carbon as taught by Kubo to adjust the lattice constant to a desired level for relaxing the strain in the substrate and ultimately improving the reliability of the device.

In re claim 79, Currie discloses [0077] that the first transistor is a PMOS transistor and the second transistor is an NMOS transistor.

In re claim 80, Kubo et al. shows (fig. 1) that an additional third semiconductor layer (14p or 14n) may comprises an alloy of silicon, germanium, and carbon.

Response to Arguments

Applicant's arguments filed with respect to claims 1-9, 12, 14, 16-17, 22-23, 25-34, 36-38, 40-42, 45-55, and 78-80 have been fully considered but they are not persuasive. The applicant primarily asserts that the motivation to combine Kubo with the prior art references is not proper because Kubo's motivation teaches away from the applicant's invention. The examiner believes that the motivation is proper and that the cited references show all of the elements of the claims. As stated in the rejection above, Kubo was cited to cure the deficiencies of the references by disclosing a semiconducting material comprising Si, Ge, and C. Although the applicant uses the material to cause lattice mismatch and Kubo uses the material to prevent lattice mismatch, Kubo is still recognized as a proper reference having proper motivation. Kubo was primarily cited to show that Si, Ge, and C were used to adjust the lattice constant of a semiconductor to a desired level. The applicant's materials of Si, Ge, and C are not novel since Kubo already teaches that these materials can adjust the lattice constant of the semiconductor. The applicant has merely discovered a new use for the material (adjusting the lattice constant to cause mismatch) and such discovery does not render the claims patentable. Therefore the cited references show all of the elements of the claims and this action is made final.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MEW
MEW
May 30, 2006

KENNETH PARKER
SUPERVISORY PATENT EXAMINER